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QUESTION BANK (DESCRIPTIVE)

Subject with Code : LPVD(16EC5709) **Branch & Specialization**: M.Tech – VLSI

Year & Sem: I-M.Tech & II-Sem **Regulation:** R16

UNIT –I

LOW POWER DESIGN, AN OVER VIEW & MOS/BiCMOS PROCESSES

1a) What are the various limitations of Low-voltage, Low-power design [5M]

b) Explain about Silicon-on-Insulator(SOI) technology [5M]

2 a) Describe triple diffused (3D) BiCMOS process with neat sketch [5M]

b) Draw the structure of Twin-well BiCMOS process and explain the same [5M]

3. Explain High-performance, High-cost digital p-well CMOS process [10M]

4 a) What are the BiCMOS manufacturing and Integration considerations [6M]

b)What are the advantages in the production of Graded-Drain structures [4M]

5) Draw the Retrograde-well CMOS process with neat diagrams. Explain how susceptibility to latch up and punch through is reduced. [10M]

6 a) Explain about punch through in short – channel MOSFETS. [5M]

b) Describe different process considerations for Bipolar transistors [5M]

7. Explain the following Isolation techniques in BiCMOS transistors

a) Junction isolation in the SBC process [5M]

b) Oxide-isolated Bipolar transistors [5M]

8. Briefly describe LOCOS isolation technique in MOS transistors with neat sketch [10M]

9. Explain the following with neat diagrams

a) Shallow trench Isolation [5M]

b) Deep trench Isolation [5M]

10. What are the considerations for integrated Analog/digital BiCMOS process [10M]

UNIT-II

LOW-VOLTAGE/LOW POWER CMOS/ BiCMOS PROCESSES & DEVICE BEHAVIOR AND MODELING

1) With the help of neat sketches explain about Polysilcon Emitter High- performance BICMOS structures and explain about the process steps. [10M]

2 a) What are the steps in implementing copper metallization in deep sub micron process? Explain. [5M]

b) Explain BSIM2 and BSIM3 spice models [5M]

3. What are the fabrication process steps for Low-voltage/Low-power SOI CMOS [10M]

4 a) Explain Lateral BJT on SOI [6M]

b) What are the limitations of the MOSFET characteristics? [4M]

5 a) What are the future trends and directions in CMOS/BICMOS processes? Explain. [6M]

b) Briefly explain LEVEL4 MOSFET Spice model [4M]

6. Describe the following two advanced MOSFET models

a) HSPICE level 50 (Philips MOS 9) model. [5M]

b) EKV MOSFET model [5M]

7. Explain the following Bipolar spice models

a) Ebers-Moll model [5M]

b) Modified Gummel-Poon Model [5M]

8. Explain the various features of HICUM transistor Model [10M]

9 a) Explain the MOSFET in a hybrid-mode environment [5M]

b) Explain the static characteristics of a MOSFET transistor [5M]

10 a) Describe briefly about VBIC95 Bipolar spice model [5M]

b) Explain the Noise model of HSPICE Level 50 [5M]

UNIT III

CMOS AND Bi-CMOS LOGIC GATES & LOW- VOLTAGE LOW POWER LOGIC CIRCUITS

1. Describe about the following conventional logic gates
   a) CMOS and [5M]
   b) BiCMOS [5M]

2 a) Draw the circuit for Full Swing complimentary MOS / Bipolar logic circuit for two input NAND gate and explain its operation. [6M]

b) Draw the circuit for High performance complimentary coupled BICMOS three input NAND and explain its working. [4M]

3a) Explain the Merged BiCMOS digital circuits and evaluate its performance [5M]

b) With a neat sketch, Explain the FS-CMBL with Feedback circuit and its features [5M]

4. Describe the operation of Quasi-complimentary BiCMOS digital circuits and analyse its performance [10M]

5 a) Explain Full swing BiCMOS/BiNMOS Digital circuits employing schottky diodes [5M]

b) Explain FS-Multidrain/Multicollector Complementary BiCMOS Buffers with a neat diagram [5M]

6. Explain feedback-type BiCMOS digital circuits [10M]

7. Describe the operation of High beta BiCMOS digital circuits and analyse its performance [10M]

8. Explain the following Bootstrapped-type BiCMOS digital circuits [10M]
   a) 1.5V logic gate [5M]
   b) Full swing Inverter [5M]

9a) Explain BiNMOSs version of Bootstrapped circuit with neat sketch [5M]

b) What are the design considerations of 1.5V Bootstrapped Full swing BiCMOS/BiNMOS inverter [5M]

10 a) Explain the working of twin capacitor BiNMOS logic gate and evaluate its performance [5M]

b) Describe ESD-free BiCMOS digital circuits and perform its comparative evaluation [5M]

UNIT –IV

LOW POWER LATCHES AND FLIP FLOPS

1a) Explain about the pipelining theme and high performance and low power theme for latches and flip flops. [5M]

b) What are setup time and hold times? Explain the MOCF and setup time and hold time considerations. [5M]

2a) Explain the need for Low-power latches and flipflops [5M]

b) Describe the evolution of latches and flipflops [5M]

3a) Describe various quality measures for latches and flipflops [5M]

b) Briefly explain single-edge triggered flipflops with neat sketch [5M]

4a) Explain double-edge triggered flipflops with neat sketch [6M]

b) Explain different power dissipation measures [4M]

5a) Describe static and semistatic flipflops with neat diagrams [6M]

b) What is meant by Synchronous theme of Flipflops [4M]

6. Explain High-performance and Low power theme of CMOS [10M]

7. Explain the following terms:

a) MOCF [5M]

b) Clock skew [5M]

8. What is the principle of operation of DETFF2 [10M]

9a) How to calculate power dissipation of a latch [5M]

b) Explain Dynamic Flipflops [5M]

10. Explain the following performance measures of a latch/flipflop

a) Full swing Considerations [5M]

b) MOCF [5M]

UNIT V

SPECIAL TECHNIQUES

1a) What is meant by clock ? Why is it required ?	[5M]
b) Explain various power reduction techniques in clock networks	[5M]
2. Briefly describe CMOS Floating node	[10M]
3. Explain various delay balancing techniques with a neat sketch	[10M]
4a) Explain different low power techniques for SRAM	[5M]
b)What is SRAM ? Draw the circuit of SRAM	[5M]
5a) What is meant by Clock Distribution Network	[5M]
b)What is Resonant clocking	[5M]

Prepared by: **S.SRUTHI**.